REMARKS

Claims 43-66, 98-103, 106 and 107 are pending in this application.

Claims 50-52, 56, 98-100 and 102, 106 107 have been amended.

Reconsideration is requested.

The Rejections Under 35 USC §132 and §112:

The amendment filed 12/4/01 has been objected to under 35 USC §132 as introducing new matter into the disclosure.

Applicants respectfully traverse.

In determining a sufficiency of a disclosure at the time an application is filed, an invention claimed should be fully capable of being reduced to practice (i.e., that no technological problems, the resolution of which would require more than ordinary skill and reasonable time, remain in order to obtain an operative, useful embodiment.) See In re HAWKINS, 179 USPQ 157, 161 (CCPA 1973).

Furthermore, the court has recognized that

> An application for a patent when filed may incorporate "essential material" by reference to (1) a United States patent, or (2) an allowed U. S. application, subject to the conditions set forth below. "Essential material" is defined as that which is necessary to (1) support the claims, or (2) for adequate disclosure of the invention (35 U.S.C. 112). "Essential material" may not be incorporated by reference to (1) patents issued by foreign countries, to (2) nonpatent publications, or to (3) a patent or application which itself incorporates "essential material" by reference. * * *
>
> The filing date of any application wherein essential material is incorporated by reference to a foreign patent or to a publication will not be affected because of the presence of such reference. In such a case, *as well as any other case which is not entitled to incorporate essential material by reference*, the applicant will be required to amend the disclosure to include the material incorporated by reference. The amendment must be accompanied by an affidavit or declaration executed by the applicant, or his attorney or agent of record, stating that the amendatory material consists of the *same* material

incorporated by reference in the referencing application. Id., citing MPEP §608.01(p).

Applicants submit that the amendatory material filed 12/4/01 for inclusion into the specification of the present application corresponds to material of incorporated U.S. Patent Nos. 4,895,810 and 5,262,336. Because material incorporated by reference may form part of an application, the disclosures of U.S. Patent Nos. 4,895,810 and 5,262,336, which are incorporated by reference within the present application, form a part of the application as though filed directly therein. Thus, applicants submit that the body of the specification may be amended to insert material of the incorporated references and that such material does not constitute new matter.

In the amendment filed 12/4/01, applicants referenced a rejection of the Examiner to certain claims under 35 USC §112, first paragraph. In the event the Examiner was implying a possible "essential matter" issue, applicants chose to amend the text of the present specification to copy portions of the material incorporated by reference into the text of the specification. Additionally, the remarks of the applicants within the amendment filed 12/4/01 expressed that such amendments were made to expressly recite at least some of the incorporated material within the text of the specification.

Accordingly, applicants again submit that the amendments to the specification as filed 12/4/01 include portions of the incorporated applications, and that they therefore do not introduce new matter.

Regarding the Examiner's disapproval of the substitute sheets of drawings, filed 2/4/01, as not supported by the showing of drawings of Figs. 6B and 6C; applicants again submit herewith that the specification included material of incorporated U.S. Patent Nos. 4,895,810 and 5,262,336. Therefore, material of U.S. Patent Nos. 4,895,810 and 5,262,336, including drawings thereof, may be deemed as much a part of the application as filed as if repeated in the application as filed. Furthermore, applicants additionally point out that amendments may be made to provide conformity between drawings and a specification and visa versa. Accordingly, applicants submit that the drawings of Figs. 6B and 6C constitute a part

of the specification, not only previously when they were incorporated by reference but also currently as copied into the specification.

Claims 44, 45, 46, 65, 66 are rejected under 35 USC §112, first paragraph, as containing subject matter which was not described in the specification in such a way as to enable on skilled in the art to which it pertains, or with which it is most nearly connected, to make and/or use the invention.

Applicants respectfully traverse.

Regarding the Examiner's statements concerning the location of insulating layer over a gate conductor, applicants submit that the specification shows insulating layers over a gate conductor. For example, the present specification shows embodiments with insulating layers 68, 168 in Figs. 13, 19 respectively, and as described in the specification with reference thereto. Further, other embodiments include an insulating layer 272 as shown in Fig. 6C and as described in the specification with reference thereto.

Furthermore, and alternatively, the claims presently set forth claimed interrelationships between various elements without setting forth unnecessary details, which would be obvious to one skilled in the art. A patent application need only contain a full description of the invention and particularly point out and distinctly claim a part, improvement, or combination which is claimed as the invention. Even if examples were missing, a mere failure to recite a detail essential to the operation does not invalidate the claims if the skill of the art can supply the detail or if the detail is shown in the specification. See *The Davis Co. v. Hemphill Co.*, 86 F. Supp. 188, 190, 83 USPQ 63,65 (M.D. N.C. 1949), (citing *Deering v. Winona Harvester Works*, 155 U.S. 286 (1894).

Applicants argue similarly with reference to the upper metal layer over the insulating layer and contacting the gate conductor through a via in the insulating layer. The present application incorporates by reference U. S. Patent No. 5,262,336, which provides exemplary such structures. Additionally, the specification at page 14, lines 19-27, discloses that in a remainder of processing, in accordance with a given embodiment, fabrication may follow conventional methods to be described generally. For example, frontside metal 94 may extend downwardly into particular trenches to form conductive source contacts which vertically short together the source and body

layers 86, 90, referencing FIG. 12. Completion steps also include opening gate contact vias at discrete locations, which can be done in this process without critical alignment, and passivating the surface. Accordingly, exemplary structures have been disclosed for supporting formation of upper metal contacting underlying structures through an insulating material.

Additionally, U.S. Patent No. 5,262,336 teaches exemplary formation of such insulating layer over trench structures and formation of upper metal over the insulating layer with contacts to regions therebelow. With respect to such description, applicants submit that once trench structures (with or without metal patterning therein) have been formed, not only is the disclosure of page 14 of the specification of the present application are available for describing completion procedures, but also procedures of incorporated U.S. Patent No. 5,262,336 would similarly be applicable for completion of upper metal layers over insulating layer with contacts to respective underlying gate or source regions or trench structures.

OK

Finally, applicants further submit that a mere failure to recite a particular detail would not render a claim invalid if one skilled in the art can supply the detail or if the detail is shown in the specification. *The Davis Co., supra.*

Because the specification includes exemplary embodiments for the claimed subject matter and the claims need not include unnecessary details, applicants submit that the specification and claims 44, 45, 46, 65 and 66 fulfill requirements of 35 USC §112, first paragraph.

Applicants similarly traverse in aggregate the various rejections of claims 44-46, 60-66, 98, 99-103, 106 and 107 under 35 USC §112, first paragraph, for reasons similar to those presented above relative to claims 44, 45, 46, 65 and 66.

Additionally, applicants note that while the specification may recite particular embodiments, such exemplary embodiments need not restrict the scope of the pending claims. As noted before, the claims need not include unnecessary details.

The Examiner asserts that the specification at page 11, lines 27 to page 17, line 1 discloses that the "gate metal layer comprises a refractory metal." Applicants traverse. Applicants respectfully quote this portion of the specification as follows: "a silicide can be formed in the remaining polysilicon material at this step to further

not OK

reduce gate resistance, for example, by refractory metal deposition and silicide formation." As set forth therein, "silicide" is not referenced as "a metal layer." not true

Accordingly, applicants submit that the present claims, including 44-46, 60-65, 98, 99-103, 106 and 107, meet the requirements of 35 USC §112, first paragraph.

Claims 50-52, 99, 106 and 107 are rejected under 35 USC §112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicants regards as the invention. While applicants submit that these claims were sufficiently definite to point out and distinctly claim the subject matter which applicants regard as the invention, amendments to form have been made, nonetheless, in an effort to advance this case to issuance.

Claim 50 has been amended to remove language "at least one."

Claim 51 has been amended to remove language "at least"; and to replace "each" with "each of the first and second ones."

Claim 98 has been amended to recite "a doped polysilicon layer" and "a metal layer disposed substantially coextensively ... ."

Claim 99 has been amended to recite "a metal layer" and to identify the metal as aluminum and the location of the silicide between the polysilicon layer and the aluminum.

Relative to claims 106 and 107, these claims have been amended for antecedence as noted by the Examiner.

Accordingly, it is submitted that these claims meet the requirements of 35 USC §112, second paragraph.

The Rejections Under 35 USC §103

Claims 43, 47, 48, 50, 51, 53, 57, 58, 61 and 63 were rejected under 35 USC §103(a) as being unpatentable over Sakamoto.

Sakamoto teaches of an insulated gate semiconductor device having a gate electrode embedded in a groove that is formed on a primary surface of a semiconductor foundation. Source and body regions are formed self-aligned with the

gate electrode. A source electrode connects the source and body regions. See the translation of Sakamoto H3-109775, page 1, lines 7-15.

Sakamoto further teaches the source electrode extended to the drain region and a Schottky diode that may be incorporated between the source and the drain to provide an advantage of reduced minority carriers in the drain region for improving high speed switching and breakdown strength. Id., page 4, lines 28-33. Additionally, Sakamoto teaches selectively forming a silicide layer on top of a polycrystalline silicon layer for the purpose of reducing the resistance of the gate. Id., page 5, lines 16-19, referencing Fig. 2(b).

After siliciding the gate polysilicon, Sakamoto teaches forming new oxide layer 10 and also P-type and N-type diffusion layers 12. Id., page 5, lines 26-29, referencing Fig. 2(c). Applicants submit that the processes for the selective oxidations and the diffusions for the formation of the new oxide layer 10 and/or P-type and N-type layers 11,12 (id, page 7, lines 28-30, referencing Fig. 4(c)) as taught by Sakamoto after the siliciding of the gate, would employ temperatures incompatible with certain features of claim 43 of the present application.

not OK

Claim 43 sets forth a recessed gate field effect power MOS device with a vertically-oriented channel, which comprises a gate conductor in a first trench. The gate conductor comprises doped polysilicon and a gate metal layer coextending over the doped polysilicon within the trench.

Sakamoto provides no disclosure of a metal layer over doped polysilicon of a gate conductor to a field effect power MOS devise with a vertically-oriented channel as set forth in claim 43. In fact, even while Sakamoto discloses an aim for "high switching speed" (Sakamoto, translation, page 4, lines 28-33), Sakamoto teaches a silicide over the gate polysilicon. Furthermore, applicants submit that the oxidation and diffusion procedures taught by Sakamoto after the formation of the gate would be incompatible with provision of a metal layer coextensively over polysilicon for a gate conductor in a trench as set forth in claim 43. Applicants submit, therefore, that the disclosure of Sakamoto teaches away from the device as set forth in claim 43.

not OK

Because Sakamoto does not disclose or suggest and provides teachings incompatible with or teaching away from features of claim 43 applicants submit that

claim 43 is patentable over Sakamoto. Likewise, it follows that dependent claims 44-66 also are patentable, at least for reason of being dependent upon allowable base claim 43 and also for their own features.

In the fourth paragraph on page 6 of the Office Action, the Examiner states that "it would have been obvious for the gate metal layer to comprise plateable metal since it has been held to be within the general skill of a worker in the art to select a known material on the basis of its suitability for the intended use as a matter of obvious design choice." Applicants respectfully traverse. Should the Examiner choose to maintain this assertion, applicants respectfully request objective evidence or an Examiner's affidavit or declaration regarding such obviousness of "plateable metal" for the devices as set forth in claims 61 and 63, to which applicants may further respond. Again, Sakamoto offers no disclosure or suggestion of providing a metal layer, let alone a "plateable metal," over a gate polysilicon in a field effect power MOS device as set forth in claims 61 and 63. Further, Sakamoto does not suggest how such "plateable metal" could be integrated therewith. In fact, Sakamoto's teachings of silicide, new oxide and diffusion processes after the gate formation seem incompatible and suggesting away from features as set forth in claims 61 and 63.

OK

Claims 44-46, 52, 55 and 56 are rejected under 35 USC §103(a) as being unpatentable over Sakamoto in view of Bulucea et al.

Claim 44, dependent on claim 43, further sets forth an insulating layer over the gate conductor, and an upper metal layer over the insulating layer and contacting the gate conductor through a via in the insulating layer.

Bulucea teaches a power MOSFET with growth of gate oxide at various trench corners. Referencing Fig. 31A, polysilicon layer 36a in a trench provides a gate electrode. A metallization layer 43 over the upper surface of the structure is patterned to define separate regions 43b (gate) and 43b (source/body) to separate gate and source/body contacts. Column 13, lines 53-59.

Applicants submit that Bulucea discloses nothing further to Sakamoto for teaching of a metal layer co-extensive over polysilicon for a gate conductor within a trench of a field effect power MOS devise as set forth in claim 44, which is dependent

on base claim 43. Let alone, such metal layer of the gate conductor within a trench and, additionally, an upper metal layer thereover as set forth in claim 44. Indeed, Bulucea teaches away from such structure by disclosing a polysilicon layer alone to structure a gate electrode in a trench. Additionally, it is submitted that Bulucea suggests no need for improvements thereof nor of looking to Sakamoto for such improvement, or vice versa of Sakamoto looking to Bulucea.

not OK

Bulucea teaches a metal layer contacting a portion of a polysilicon layer outside the trench of the gate structure and over a field region. Applicants submit, however, that there is no disclosure or suggestion in Bulucea and/or Sakamoto, singularly, or taken together, to provide for the features of the present invention, including the metal layer coextending over the gate conductor within a trench and the upper layer of metal to the field effect power MOS device with the vertically-oriented channel as set forth in claim 44.

not OK

Finally, neither Sakamoto nor Bulucea disclose a metal layer over a gate polysilicon of a gate conductor in a trench; therefore, it cannot be said that a combination thereof would suggest such features to a field effect power MOS devise with the vertically-oriented channel as set forth in claim 44.

not OK

Accordingly, applicants submit that claim 44, dependent on base claim 43, is patentable over Sakamoto and Bulucea either singularly or taken together. Likewise, dependent claims 45-46, 52, 55 and 56 are submitted as being patentable over Sakamoto and Bulucea for reasons similar to the patentability of claim 44, and also for their own features.

not OK

Claims 60, 62, 64, 65 and 66 are rejected under 35 USC §103 as being unpatentable over Sakamoto in view of Bulucea, further in view of Temple. Applicants respectfully traverse.

Claim 60, dependent on claim 43, further defines the gate metal layer as comprising aluminum.

Temple discloses gate structures of conventional MOSFET devices on a substrate. The devices comprise polysilicon over an upper surface of a substrate and silicide and metallization over the polysilicon gate. There is no disclosure or

suggestion that the metal and polysilicon gate structure of Temple could be used for a gate conductor in a trench of a field effect power MOS devise of a vertically-oriented channel as set forth in claim 44. Indeed, despite the teachings of Temple, Sakamoto discloses selective silicide formation on polysilicon for a gate structure and Bulucea teaches of a polysilicon layer. Therefore, relative to the art of power MOS devices of vertically-oriented channels, applicants submit that the teachings of Sakamoto for simple silicide over polysilicon silicide and the teachings of Bulucea for only a polysilicon layer for respective gate structures, especially in view of the availability of Temple, further suggests that Sakamoto and Bulucea teach away from the features of certain embodiments of the present invention and as set forth in claim 60.

Applicants further point out that Temple is of the art of lateral channel devices. In contrast, claim 60 addresses a vertically-oriented channel type field effect power MOS device which comprises a gate structure in a trench. Applicants submit that an artisan dealing with vertically-oriented channel devices of Sakamoto or Bulucea would not find motivations to explore Temple for developing new combinations thereof with Sakamoto or Bulucea, let alone, to establish a vertically-oriented channel device as set forth in claim 60.

Additionally, and similar to the arguments in favor of claim 43 and 44, applicants submit that the oxidation and diffusion procedures of Sakamoto to form the insulating materials and diffusion regions after forming the gates would be incompatible with provision of an aluminum layer coextensively over polysilicon for a gate conductor within a trench of a field effect power MOS device as set forth in claim 60. Thus, applicants submit that Sakamoto's teachings of simple silicided polysilicon gate structures teach away from features of claim 60.

OK

It is not enough that a series of various references of a variety of fields may provide a catalog of elements to possible embodiments. For obviousness, there must be some reason, suggestion, or motivation within the references to provide foundation to those of ordinary skill in the art, which would clearly and particularly lead one of ordinary skill in the art toward their combination. "It is impermissible to use the claimed invention as a . . . 'template' to piece together the teachings of the prior art so that the claimed invention is rendered obvious. . . . 'One cannot use hindsight reconstruction to pick and choose among isolated disclosures in the prior art to

deprecate the claimed invention.'" *In re Fritch*, 972 F.2d 1260, 1266, 23 USPQ2d 1780, 1784 (Fed. Cir. 1992). Piecing together art from various unrelated fields in an attempt to reconstruct the invention is an impermissible use of hindsight.

Accordingly, it is submitted that claim 60 is patentable over Sakamoto, Bulucea and Temple, either singularly or taken together. Likewise, claims 62, 64, 65 and 66 are submitted as being patentable over the prior art for reasons similar to those in favor of the patentability of claim 60, and additionally for their own features.

OK

Claims 49 and 54 are rejected under 35 USC §103(a) as being unpatentable over Sakamoto in view of Davies. Applicants respectfully traverse.

The Examiner describes Davies as a vertical MOSFET. The MOSFET of Davies may allow carriers to move vertically therein - e.g., from the drain electrode 24 to the drain region just beneath gate oxide 12 referencing Fig. 1. However, channel regions 20 comprise lateral channels.

Claims 49 and 54 are directed to field effect power MOS devices of vertically-oriented channels.

Applicants submit that an artisan in the field of vertically-oriented channel regions may not look to the teachings of Davies, nor be motivated thereby, for establishing combination with Sakamoto, let alone, a recessed gate vertically-oriented channel device as set forth in claims 49 and 54.

Additionally, and similarly as set forth earlier herein relative to claim 44, applicants submit that Davies lends nothing further to the disclosure of Sakamoto to disclose of a metal layer co-extensive over polysilicon for a gate conductor within a trench for a recessed gate field effect power MOS devise with a vertically-oriented channel as set forth in claims 49 and 54.

Accordingly, it is submitted that claims 49 and 59 are patentable over the prior art.

not OK

Claim 59 is rejected under 35 USC §103(a) as being unpatentable over Sakamoto in view of Blanchard.

Again, applicants submit that Blanchard adds nothing further to the disclosure of Sakamoto for suggesting a metal layer coextensively over polysilicon for a gate conductor in a trench of a recessed gate field effect power MOSFET device having a vertically-oriented channel as defined in claim 59. In fact, applicants submit that Blanchard provides further evidence of the non-obviousness of such metal layer over polysilicon for the gate conductor thereof. Indeed, Blanchard teaches away from a metal layer coextensively over polysilicon of a gate conductor in a trench to a recessed gate field effect power MOS devise with a vertically-oriented channel as set forth in claim 59.

Blanchard discloses a gate of polysilicon in a groove. Blanchard further teaches that the gate may, alternatively, comprise silicide. See column 5, lines 37-48. After forming such polysilicon or silicide gate, Blanchard further discloses oxidization to consume a portion of polysilicon layer 33 in groove 31 until the top surface of the oxidized portion 35 above gate 34 forms an essentially flat surface. Column 5, lines 65-68.

Applicants submit that a metal layer coextensively over polysilicon in a trench, as set forth by embodiments of the present invention, would not be agreeable with the teachings of Blanchard. Such a metal layer would prevent oxidization of an upper portion of silicon of the gate to form a flat surface as taught by Blanchard. Furthermore, applicants submit that such oxidation temperatures may be incompatible with such metal layer. Accordingly, applicants submit that Blanchard teaches away from features of the present invention.

Because Blanchard and Sakamoto, either singly or together, do not disclose or suggest, and in fact, teach away from features of the present invention, as set forth in claim 59, applicants submit that claim is patentable over the prior art.

not OK

Metal Layer Coextensively Over Polysilicon of Gate Conductor

Exemplary embodiments of the present application, as claimed herein, set forth a metal layer over polysilicon for the gate conductors. In other alternative embodiments, silicide may be formed over silicon or polysilicon and a metal layer then formed on top of this layer. As used herein, metal layer shall be distinguished from silicide, which is a reaction compound of silicon. For example, as set forth in

claim 62, dependent on claim 43, the gate conductor comprises gate metal coextending over doped polysilicon in a trench and a refractory metal silicide may be formed at the surface of the doped polysilicon and beneath the gate metal layer. Accordingly, applicants respectfully traverse the Examiner's assertion of page 10, lines 2-4 of the Office Action.

not true

Formation of Upper Metal Layer Over Insulative Layer Supported by the Specification

The present application incorporates by reference U. S. Patent No. 5,262,336. Additionally, the specification at page 14, lines 19-27, discloses in accordance with a given embodiment, that later processing steps may follow conventional methods and be described generally. For example, frontside metal 94 may extend downwardly into particular trenches to form conductive source contacts that vertically short together the source and body layers 86, 90, referencing FIG. 12. Additionally, the metal extending into these trenches to form source contacts may contact a top surface of a P-type layer 26" at the bottom of the trench. The specification further discloses that the completion steps may include opening gate contact vias at discrete locations, which can be done in this process without critical alignment, and passivating the surface. Accordingly, applicants submit that the specification discloses a structure and provides basis for the formation of upper metal contacting underlying structures through insulating material.

OK

Additionally, U.S. Patent No. 5,262,336 teaches exemplary formation of such insulating layer over trench structures and formation of upper metal over the insulating layer with contacts to regions therebelow. Applicants submit that once trench structures (with or without metal patterning therein) have been formed, not only the disclosure of page 14 of the specification of the present application are available for describing such completion procedures, but that also procedures of U.S. Patent No. 5,262,336 would similarly be applicable for the completion steps associated with forming upper metal layers over insulating layer with contacts to respective underlying gate or source regions or trench structures thereof. Accordingly, applicants respectfully traverse the Examiner's assertions of page 10, lines 5-13 of the Office Action.

planar MOSFET

OK

Furthermore, applicants submit that claims 46 and 60-65 find support in the specification of the present application, which includes material incorporated by reference. Accordingly, applicants traverse the Examiner's assertion (page 10, lines 14-

15) concerning U.S. Patent Nos. 4,895,810 and 5,262,336 teaching subject matters of claims 46 and 60-65. It may be noted, for example, that these claims depend on base claim 43. Applicants submit that support for all claims of the present application may be found in the specification of the application, which includes subject mater incorporated by reference. Plainly, following these teachings, it is readily apparent how to form a metal (aluminum) layer on the upper surface of the polysilicon.

Claims of the Present Application Supported by the Specification

Applicants generally traverse further statements of the Examiner, e.g., including those of page 10, line 21 to page 11, line 7 of the Office Action of May 22, 2002.

Applicants respectfully point out that the present specification includes disclosure of isolation layer 68 over conductive material 62 in certain trenches. See page 12, lines 1-3. This aside, applicants again note that the present specification includes the disclosures of U.S. Patent Nos. 4,895,810 and 5,262,336, which are incorporated by reference.

Claim 66, which depends on base claim 44, sets forth insulating material as comprising at least one of oxide, nitride, oxy-nitride, glass and phosphosilicate glass. Applicants submit that such exemplary insulating layer finds support within the specification of the present application.

Finally, claim 98 sets forth a power MOSFET device, which may include an insulating layer disposed over a gate structure, that comprises a doped polysilicon layer and a metal layer disposed substantially coextensively over the doped polysilicon layer. Metallization is disposed over the insulating layer and contacts the gate structure through the insulating layer. The Examiner asserts that the last two paragraphs of claim 98 are not supported by U.S. Patent No. 4,895,810. Applicants respectfully traverse and submit that the features of claim 98 find support in the specifications of U.S. Pat. Nos. 4,895,810 and 5,262,336. Indeed in U.S. Patent No. 5,262,336 at columns 15-16 and Figs. 18-19, clear support for a second metal layer connecting to a first metal layer, through an insulating layer.

In *In re Kaslow and Uniform Product Code Council, Inc.*, 217 USPQ 1089, 1096 (CAFC 1983), the court set forth that "the test for determining compliance with the written description requirement is whether the disclosure of the application as

originally filed reasonably conveys to the artisan that the inventor had possession at that time of the later claimed subject matter, rather than the presence or absence of literal support in the specification for the claim language."

The specification of U.S. Patent No. 4,895,810 recites that when layer 72 comprises a material that can remain on the device surface, such as glass, that its removal is not necessary. See column 11, lines 14-16, referencing Fig. 16C-16D. At column 10, lines 56-64, the specification of '810 describes an exemplary material for layer 72, such as polyimide or spin-on glass and that it may be applied using spin, spray, or roll-on techniques. Applicants have found such material coatings to be compatible with a metal layer over polysilicon of the gate structure.

As to a metallization after the insulating layer, applicants submit that an artisan of ordinary skill in the art would understand provision of such metallization to contact the gate structure. To hold otherwise would present an absurdity of forming a device encapsulated within glass, isolated from external electrical interfacing. Furthermore, the '810 specification at column 1, lines 28-30, recognizes metallization steps of the prior art as may be associated with multiple layering techniques.

OK

As established by the court in *Stearn v. Superior Distributing Company et al.*, 215 USPQ 1089, 1093 (CA 6 1982), "new matter is not introduced by amendments, continuation applications, or continuations in part that merely clarify or make definite that which was expressly or inherently disclosed in [a] parent application or that conform[s the] specification to matter originally disclosed in drawings or claims; added subject matter is not new matter when it is something that might fairly be deduced from the original application."

OK

Accordingly, because the description discloses leaving an insulating layer over the gate structure, and would inherently be understood to include metallization over such insulating layer for allowance of electrical interfacing to the gate structure (and as is explicitly taught in U.S. Patent No. 5,262,336); applicants submit that the specification reasonably conveys sufficient details to enable an artisan skilled in the art to practice the invention and understand that the inventor had possession of this claimed subject matter. It is submitted therefore that the specifications of U.S. Patent Nos. 4,895,810 and 5,262,336 provide ample support for these features of a power MOSFET as set forth in claim 98.

OK

OK

CONCLUSION

In view of the above, reconsideration and allowance of claims 43-66, 98-103, 106 and 107 is respectfully requested.

Applicants encourage the Examiner to contact the undersigned should the Examiner wish to discuss the substance of this application and/or amendment.

20575

PATENT TRADEMARK OFFICE

Respectfully submitted,

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ON Nov. 22, 2002
Judy Wigmore

VERSION WITH MARKINGS TO SHOW CHANGES MADE

In the specification

FIGS. 1 -12 are cross-sectional views of a portion of a silicon substrate showing fabrication of [a recessed gate field effect] power MOS devices in accordance with [a first embodiment] exemplary embodiments of the invention.

In the claims:

50. (Twice Amended) A recessed gate field effect power MOS device according to claim 43 including [~~at least one~~] a vertically-oriented sidewall spacer extending upward from the upper surface of the substrate, the [~~at least one~~] vertically-oriented sidewall spacer[s] atop [~~their respective~~] the vertically-oriented layers.

51. (Twice Amended) A recessed gate field effect power MOS device according to claim 50 including [~~at least~~] first and second ones of said vertically-oriented layer on respective sides of the trench, each of the first and second ones having one of said vertically-oriented sidewall spacer thereon, and an insulative layer extending laterally between the sidewall spacers over the gate conductor.

52. (Twice Amended) A recessed gate field effect power MOS device according to claim 51 including an upper metal layer extending over the insulative layer and the vertically-oriented sidewall spacer[s] and contacting the vertically-extending source conductor.

56. (Twice Amended) A recessed gate field effect power MOS device according to claim 43 wherein the first trench, the gate oxide layer and the gate conductor together form a gate structure configured as a finger, said recessed gate field effect power MOS device comprising a plurality of said fingers;

the source conductor intermediate the fingers of said plurality of fingers to define an interdigitated source-gate structure.

98. (Amended) A power MOSFET comprising:

a semiconductor substrate, the substrate comprising drain semiconductor material of a first dopant type;

source semiconductor material of a dopant type the same as said first dopant type;

channel semiconductor material of a second dopant type disposed between the source semiconductor material and the drain semiconductor material, the channel semiconductor material operative under field effect to conduct current between the source semiconductor material and the drain semiconductor material;

a conductive gate structure configured to enable provision of a field to the channel semiconductor material;

a gate oxide layer disposed between the conductive gate structure and the channel semiconductor material;

said conductive gate structure comprising a doped polysilicon layer contacting the oxide layer and a metal layer disposed substantially coextensively over the doped polysilicon;

an insulating layer disposed over said gate structure; and

metallization over said insulating layer, the metallization contacting the gate structure through said insulating layer.

99. (Amended) A power MOSFET according to claim 98 wherein the metal layer of the conductive gate structure comprises aluminum, the conductive gate structure further comprising [a metal on] a refractory metal-silicide between the doped polysilicon layer and the aluminum.

100. (Amended) A power MOSFET according to claim 98 wherein the metal layer of the conductive gate structure comprises plateable metal.

102. (Amended) A power MOSFET according to claim 98 wherein the [gate] metal layer comprises aluminum.

106. (Amended) A power MOSFET according to claim 98 wherein the source semiconductor material, channel semiconductor material, and drain semiconductor material are configured to define a vertically-oriented channel structure, said [vertical orientation] vertically-oriented channel structure comprising an orientation normal to an upper surface of said substrate.

107. (Amended) A power MOSFET according to claim 106, wherein the conductive gate structure comprises a laterally patterned interconnected matrix enclosing a plurality of islands, said plurality of islands comprising respective ones of a plurality of said vertically-oriented channel structure[s]; said power MOSFET further comprising source conductor extending downwardly into said plurality of islands, the source conductor contacting the source semiconductor material of respective said vertically-oriented channel structures of said plurality of islands.